

Serial No.: 10/088,988

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) ~~Method~~ A method for processing conditional jump instructions in a processor with pipeline computer architecture, the method comprising:
 - (a) loading and decoding a processor instruction, the processor instruction containing an instruction opcode, register addresses, a relative jump distance, a precondition, which specifies under which conditions the instruction is actually to be executed, and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition comprises a plurality of post-condition bits that are checked in the processor;
 - (b) execution of the decoded processor instruction if the precondition is fulfilled; and
 - (c) jumping to a jump address as a function of the relative jump distance contained in the processor instruction if the post-condition is fulfilled and the checked flag bits are set.
2. (Cancelled)
3. (Currently Amended) An apparatus for processing conditional jump instructions in a processor with pipeline computer architecture, the apparatus comprising:
 - (a) an instruction decoder for decoding a processor instruction that contains an instruction opcode, register addresses, a relative jump distance, a precondition, which specifies under which conditions the instruction is actually to be executed, and a post-condition, which specifies that a conditional jump is to be processed and the corresponding flag bits of an arithmetic-logic unit are to be checked, wherein the post-condition

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comprises a plurality of post-condition bits that are checked in the processor; and

- (b) wherein the instruction decoder is operable to check, in the case of a fulfilled precondition, whether the post-condition is fulfilled and the checked flag bits are set, if positive, driving a program counter for forming a jump address as a function of the relative jump distance contained in the processor instruction.